

CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

5 forming a first layer of epitaxial silicon above a surface of a semiconducting substrate;

forming a second layer of epitaxial silicon above said first layer of epitaxial silicon;

forming a third layer of epitaxial silicon above said second layer of epitaxial silicon;

10 forming a trench isolation region that extends through at least said third layer of epitaxial silicon; and

forming a portion of a semiconductor device above said third layer of epitaxial silicon within an area defined by said isolation region.

2. The method of claim 1, wherein said semiconducting substrate is doped with a

15 dopant material of a first type and said second and third layers of epitaxial silicon are doped with a dopant material that is of a type opposite to that of said first type of dopant material.

3. The method of claim 1, wherein said semiconducting substrate is doped with a

20 P-type dopant material and said second and third layers of epitaxial silicon are doped with an N-type dopant material.

4. The method of claim 1, wherein said semiconducting substrate is doped with

an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

5. The method of claim 1, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

6. The method of claim 1, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

7. The method of claim 1, wherein said second and third layers of epitaxial silicon are doped layers of epitaxial silicon and wherein said second layer of epitaxial silicon has a greater concentration level of dopant material than said third layer of epitaxial silicon.

8. The method of claim 1, wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor.

9. The method of claim 1, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of a P-type dopant material.

10. The method of claim 9, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of an N-type dopant material.

11. The method of claim 9, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of an N-type dopant material.

12. The method of claim 9, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of an N-type dopant material.

13. The method of claim 1, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of an N-type dopant material.

5 14. The method of claim 13, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of a P-type dopant material.

15. The method of claim 13, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of a P-type dopant material.

10 16. The method of claim 13, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of a P-type dopant material.

15 17. The method of claim 1, wherein said first layer of epitaxial silicon has a thickness of approximately 15-30 microns.

18. The method of claim 1, wherein said second layer of epitaxial silicon has a thickness of approximately 0.5-2.0 microns.

20 19. The method of claim 1, wherein said third layer of epitaxial silicon has a thickness of approximately 20-25 microns.

20. The method of claim 1, wherein forming a trench isolation region comprises:
performing at least one etching process to form a trench that extends through at least
25 said third layer of epitaxial silicon; and

forming at least one insulating material in said trench.

21. The method of claim 1, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

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22. A method, comprising:

forming a first layer of epitaxial silicon above a surface of a semiconducting substrate,
said semiconducting substrate being doped with a first type of dopant material;

forming a second layer of epitaxial silicon above said first layer of epitaxial silicon,
said second layer of epitaxial silicon being doped with a dopant material that
is of a type opposite to that of said first type of dopant material;

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forming a third layer of epitaxial silicon above said second layer of epitaxial silicon,
said third layer of epitaxial silicon being doped with a dopant material that is
of a type opposite to that of said first type of dopant material, wherein said
second layer of epitaxial silicon has a greater concentration level of dopant
material than said third layer of epitaxial silicon;

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forming a trench isolation region that extends through at least said third layer of
epitaxial silicon; and

forming a semiconductor device above said third layer of epitaxial silicon within an
area defined by said isolation region.

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23. The method of claim 22, wherein said semiconducting substrate is doped with
a P-type dopant material and said second and third layers of epitaxial silicon are doped with
an N-type dopant material.

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24. The method of claim 22, wherein said semiconducting substrate is doped with an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

5 25. The method of claim 22, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

26. The method of claim 22, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

10 27. The method of claim 22, wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor.

15 28. The method of claim 22, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of a P-type dopant material.

29. The method of claim 28, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of an N-type dopant material.

20 30. The method of claim 28, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of an N-type dopant material.

25 31. The method of claim 28, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of an N-type dopant material.

32. The method of claim 22, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of an N-type dopant material.

5 33. The method of claim 32, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of a P-type dopant material.

34. The method of claim 32, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of a P-type dopant material.

10 35. The method of claim 32, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of a P-type dopant material.

15 36. The method of claim 22, wherein said first layer of epitaxial silicon has a thickness of approximately 15-30 microns.

37. The method of claim 22, wherein said second layer of epitaxial silicon has a thickness of approximately 0.5-2.0 microns.

20 38. The method of claim 22, wherein said third layer of epitaxial silicon has a thickness of approximately 20-25 microns.

39. The method of claim 22, wherein forming a trench isolation region comprises:
performing at least one etching process to form a trench that extends through at least
25 said third layer of epitaxial silicon; and

forming at least one insulating material in said trench.

40. The method of claim 22, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

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41. A method, comprising:

performing an *in situ* epitaxial growth process in a single epitaxial reactor to form:

a first layer of epitaxial silicon above a surface of a semiconducting substrate,
said semiconducting substrate being doped with a first type of dopant
material,

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a second layer of epitaxial silicon above said first layer of epitaxial silicon,
said second layer of epitaxial silicon being doped with a dopant
material that is of a type opposite to that of said first type of dopant
material, and

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a third layer of epitaxial silicon above said second layer of epitaxial silicon,
said third layer of epitaxial silicon being doped with a dopant material
that is of a type opposite to that of said first type of dopant material,
wherein said second layer of epitaxial silicon has a greater concentra-
tion level of dopant material than said third layer of epitaxial silicon;

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forming a trench isolation region that extends through at least said second and third
layers of epitaxial silicon; and

forming a semiconductor device above said third layer of epitaxial silicon within an
area defined by said isolation region.

42. The method of claim 41, wherein said semiconducting substrate is doped with a P-type dopant material and said second and third layers of epitaxial silicon are doped with an N-type dopant material.

5 43. The method of claim 41, wherein said semiconducting substrate is doped with an N-type dopant material and said second and third layers of epitaxial silicon are doped with a P-type dopant material.

10 44. The method of claim 41, wherein said first layer of epitaxial silicon is an undoped layer of epitaxial silicon.

45. The method of claim 41, wherein said first layer of epitaxial silicon is doped with either a P-type or an N-type dopant material.

15 46. The method of claim 41, wherein forming a trench isolation region comprises: performing at least one etching process to form a trench that extends through at least said second and third layers of epitaxial silicon; and forming at least one insulating material in said trench.

20 47. The method of claim 41, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

48. The method of claim 41, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of a P-type dopant material.

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49. The method of claim 48, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of an N-type dopant material.

50. The method of claim 48, wherein said second layer of epitaxial silicon has a
5 dopant concentration greater than approximately $5e^{17}$ ions/cm³ of an N-type dopant material.

51. The method of claim 48, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of an N-type dopant material.

10 52. The method of claim 41, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of an N-type dopant material.

53. The method of claim 52, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of a P-type dopant material.

15 54. The method of claim 52, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of a P-type dopant material.

55. The method of claim 52, wherein said third layer of epitaxial silicon has a
20 dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of a P-type dopant material.

56. A device, comprising:

a substrate;

a first layer of epitaxial silicon formed above said substrate;

25 a second layer of epitaxial silicon formed above said first layer of epitaxial silicon;

a third layer of epitaxial silicon formed above said second layer of epitaxial silicon;
a trench isolation region that extends through at least said third layer of epitaxial
silicon, said trench isolation region defining an active area; and
at least one component of a semiconductor device formed in or above said third layer
5 of epitaxial silicon within said active area.

57. The device of claim 56, wherein said semiconducting substrate is doped with a
dopant material of a first type and said second and third layers of epitaxial silicon are doped
with a dopant material that is of a type opposite to that of said first type of dopant material.

10 58. The device of claim 56, wherein said semiconducting substrate is doped with a
P-type dopant material and said second and third layers of epitaxial silicon are doped with an
N-type dopant material.

15 59. The device of claim 56, wherein said semiconducting substrate is doped with
an N-type dopant material and said second and third layers of epitaxial silicon are doped with
a P-type dopant material.

20 60. The device of claim 56, wherein said first layer of epitaxial silicon is an
undoped layer of epitaxial silicon.

61. The device of claim 56, wherein said first layer of epitaxial silicon is doped
with either a P-type or an N-type dopant material.

62. The device of claim 56, wherein said second and third layers of epitaxial silicon are doped layers of epitaxial silicon and wherein said second layer of epitaxial silicon has a greater concentration level of dopant material than said third layer of epitaxial silicon.

5 63. The device of claim 56, wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor.

10 64. The device of claim 56, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of a P-type dopant material.

65. The device of claim 64, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of an N-type dopant material.

15 66. The device of claim 64, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of an N-type dopant material.

67. The device of claim 64, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of an N-type dopant material.

20 68. The device of claim 56, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of an N-type dopant material.

25 69. The device of claim 68, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of a P-type dopant material.

70. The device of claim 68, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of a P-type dopant material.

5 71. The device of claim 68, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of a P-type dopant material.

72. The device of claim 56, wherein said first layer of epitaxial silicon has a thickness of approximately 15-30 microns.

10 73. The device of claim 56, wherein said second layer of epitaxial silicon has a thickness of approximately 0.5-2.0 microns.

15 74. The device of claim 56, wherein said third layer of epitaxial silicon has a thickness of approximately 20-25 microns.

75. The device of claim 56, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

20 76. A device, comprising:
a substrate, said substrate being doped with a dopant material of a first type;
a first layer of epitaxial silicon formed above said substrate;
a second layer of epitaxial silicon formed above said first layer of epitaxial silicon,
said second layer of epitaxial silicon being doped with a dopant material that
25 is of a type opposite to that of said first type of dopant material;

a third layer of epitaxial silicon formed above said second layer of epitaxial silicon,
said third layer of epitaxial silicon being doped with a dopant material that is
of a type opposite to that of said first type of dopant material, wherein said
second layer of epitaxial silicon has a greater concentration level of dopant
5 material than said third layer of epitaxial silicon;
a trench isolation region that extends through at least said third layer of epitaxial
silicon, said trench isolation region defining an active area; and
at least one component of a semiconductor device formed in or above said third layer
of epitaxial silicon within said active area.

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77. The device of claim 76, wherein said semiconducting substrate is doped with a
P-type dopant material and said second and third layers of epitaxial silicon are doped with an
N-type dopant material.

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78. The device of claim 76, wherein said semiconducting substrate is doped with
an N-type dopant material and said second and third layers of epitaxial silicon are doped with
a P-type dopant material.

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79. The device of claim 76, wherein said first layer of epitaxial silicon is an
undoped layer of epitaxial silicon.

80. The device of claim 76, wherein said first layer of epitaxial silicon is doped
with either a P-type or an N-type dopant material.

81. The device of claim 76, wherein said first, second and third layers of epitaxial silicon are formed by performing an *in situ* epitaxial growth process in a single epitaxial reactor.

5 82. The device of claim 76, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of a P-type dopant material.

83. The device of claim 82, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of an N-type dopant material.

10 84. The device of claim 82, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of an N-type dopant material.

15 85. The device of claim 82, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of an N-type dopant material.

86. The device of claim 76, wherein said substrate has a dopant concentration of approximately $1e^{17}$ - $5e^{17}$ ions/cm³ of an N-type dopant material.

20 87. The device of claim 86, wherein said first layer of epitaxial silicon has a dopant concentration less than approximately $1e^{15}$ ions/cm³ of a P-type dopant material.

88. The device of claim 86, wherein said second layer of epitaxial silicon has a dopant concentration greater than approximately $5e^{17}$ ions/cm³ of a P-type dopant material.

89. The device of claim 86, wherein said third layer of epitaxial silicon has a dopant concentration of approximately $5e^{14}$ - $1e^{15}$ ions/cm³ of a P-type dopant material.

90. The device of claim 76, wherein said first layer of epitaxial silicon has a
5 thickness of approximately 15-30 microns.

91. The device of claim 76, wherein said second layer of epitaxial silicon has a thickness of approximately 0.5-2.0 microns.

10 92. The device of claim 76, wherein said third layer of epitaxial silicon has a thickness of approximately 20-25 microns.

93. The device of claim 76, wherein said semiconductor device comprises at least one of a bipolar transistor, a resistor, a diode, a logic device and a memory device.

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